Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

Marks

1 a) Convert the following numbers: (4)

(a) $(101111.1101)_2$ to decimal (b) $(53.625)_{10}$ to binary

b) What is the specialty of Grey code and specify how this property can be utilized in a practical application (4)

c) State the relationship between error detection ability, error correction ability and minimum distance of a code. An 8421 code is transmitted as Hamming code with even parity and the code received is 0011101. Determine the single error if any and correct it (7)

2 a) Obtain the minimal SOP expression for $\sum m(2,3,5,7,9,11,12,13,14,15)$ and implement it using NAND logic (7)

b) Using K-map, obtain the minimal sum of product of the following expression ABCD+AB'C'D'+AB'C+AB (8)

3 a) Obtain binary representation of $(-25)_{10}$ in (i) sign-magnitude (ii) 1's complement (iii) 2's complement form (5)

b) Derive expressions for the output of a 1-bit magnitude comparator and implement it using gates (10)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Differentiate between PLA and PAL with necessary diagrams (7)

b) What is the significance of (a) propagation delay (b) power dissipation (c) Fan-out of gates. Compare CMOS, ECL and TTL logic families in terms of these parameters (8)

5 a) What is race-around condition in flip-flops? How is it solved? (5)

b) Design a mod-6 synchronous counter using T-flip-flops (10)

6 a) Draw the circuit of a TTL NAND gate with totem pole output. Mention the advantages and disadvantages of totem pole configuration (7)

b) Realize a J K flip-flop using D flip-flops (8)

PART C

Answer any two full questions, each carries20 marks.

7 a) Draw a serial input parallel output (4 bit) shift register. Convert this to a ring counter using suitable modifications (10)

b) Draw the block diagram of a finite state machine. Differentiate between Mealy and Moore machine with the help of block diagrams (10)

8 a) Design a 2 bit synchronous up/down counter using D flip-flop (10)

b) Reduce the following state table using implication chart method (10)

PS	NS, z	
	X=0	X=1
S0	S4, 0	S3, 1
S1	S5, 0	S3, 0
S2	S4, 0	S1, 1
S3	S5, 0	S1, 0
S4	S2, 0	S5, 1
S5	S1, 0	S2, 0

9 a) A clocked sequential circuit with single input X and single output Y produces output Z equal to 1, whenever the input X completes the sequence 110 and overlap is allowed. Obtain the state diagram and the minimum state table. Prepare excitation table and design the circuit using D flip-flop. (10)

b) List different classes of shift registers. Illustrate the use of the use of parallel LOAD/SHIFT in shift registers (10)

****